**Pipelined Processor ID stage Lab**

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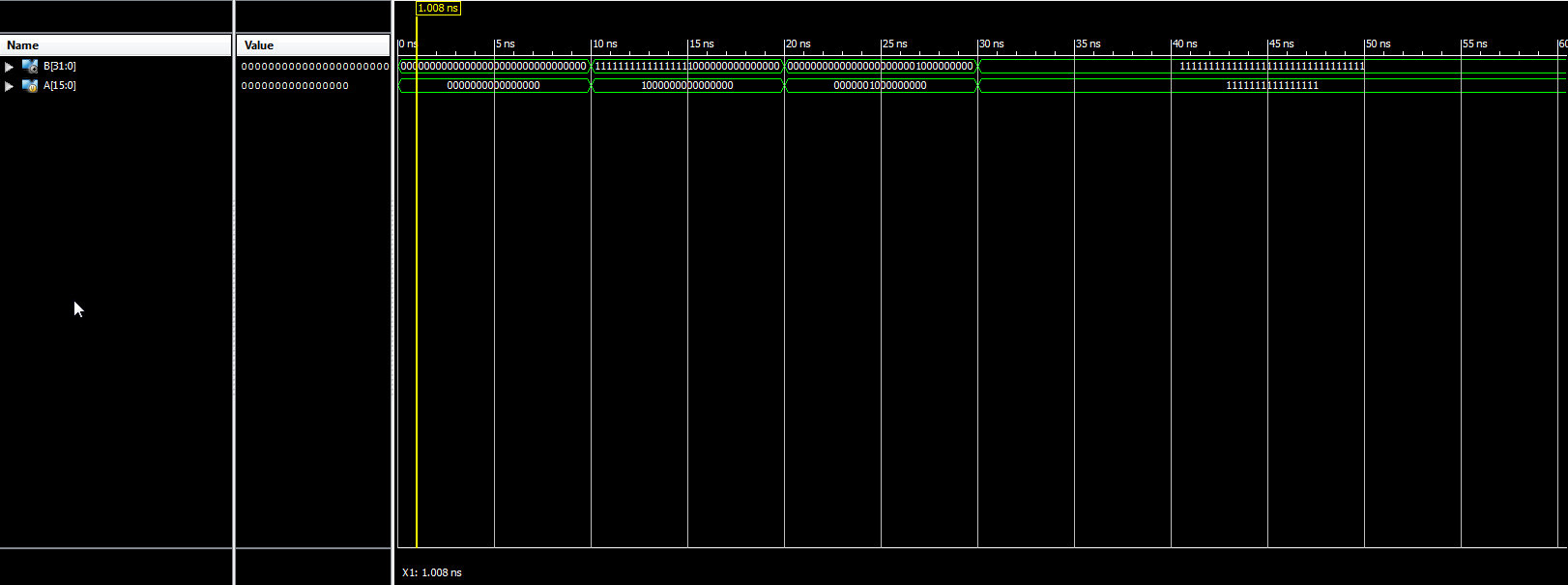
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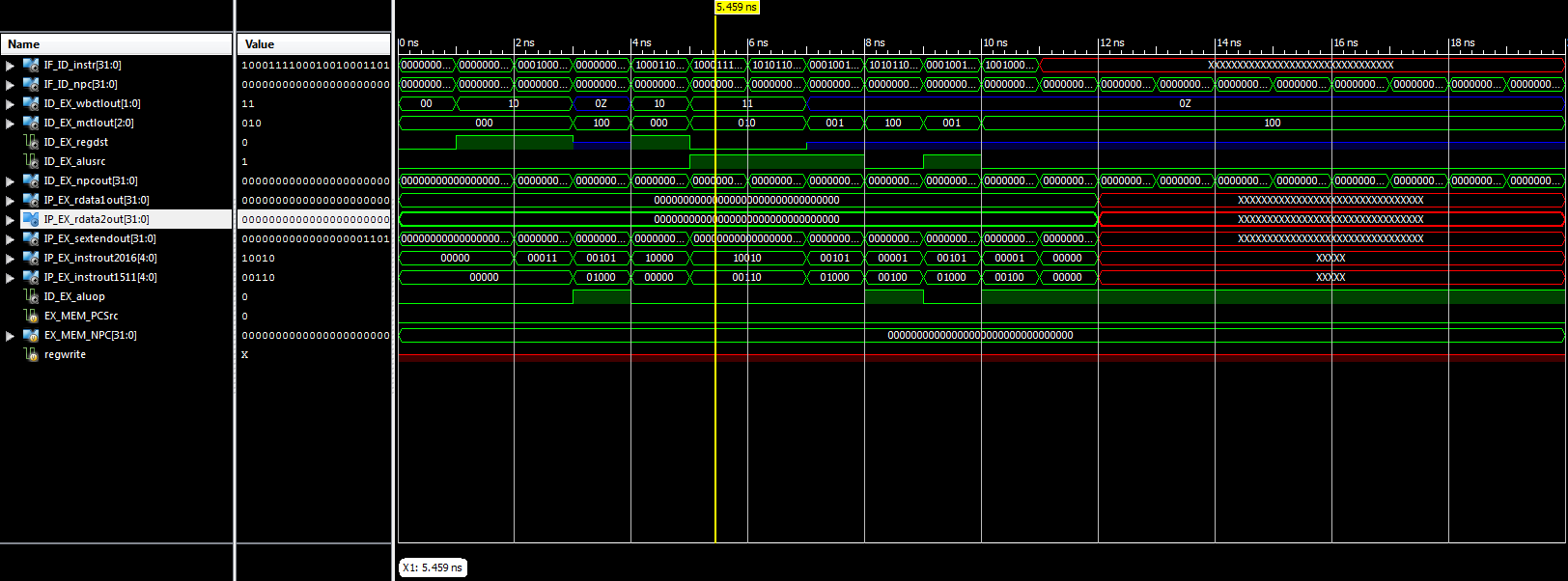
**13 January 2021**

**CSE 4010 Winter 2021**

The ID (Instruction Decode) stage decodes the instruction in the IR (Instruction Register), calculates the next PC (Program Counter), and reads any operands required from the register file. In this lab, we have two registers within the ID pipeline which are R1 and R2. These two values will be processed through the register file and will be included at the end of the ID pipeline. The control block will also access the instruction from the IF buffer and will decipher 3 separate groups of bits from the 6-bit opcode of the instruction. These groups will help distinguish them to define the Execution, Memory, and Write-Back control lines for the upcoming pipelines. Depending on the instruction type, the register destination in the register file will be stored into the ID buffer through either a sign-extended value from 16-bits to 32-bits or through its 26-bit jump value from the instruction memory.

The simulation of the test bench gives the following:





The pipeline simulation goes through the values stored in memory and interprets them as instructions, the first 9 values in memory are valid instructions given so they populate the modules with relevant instruction information, but the rest of the memory is either invalid or unstructured, resulting in the "opcode not recognized" error. The information is processed and stored in the ID buffer to be used in the EX stage.